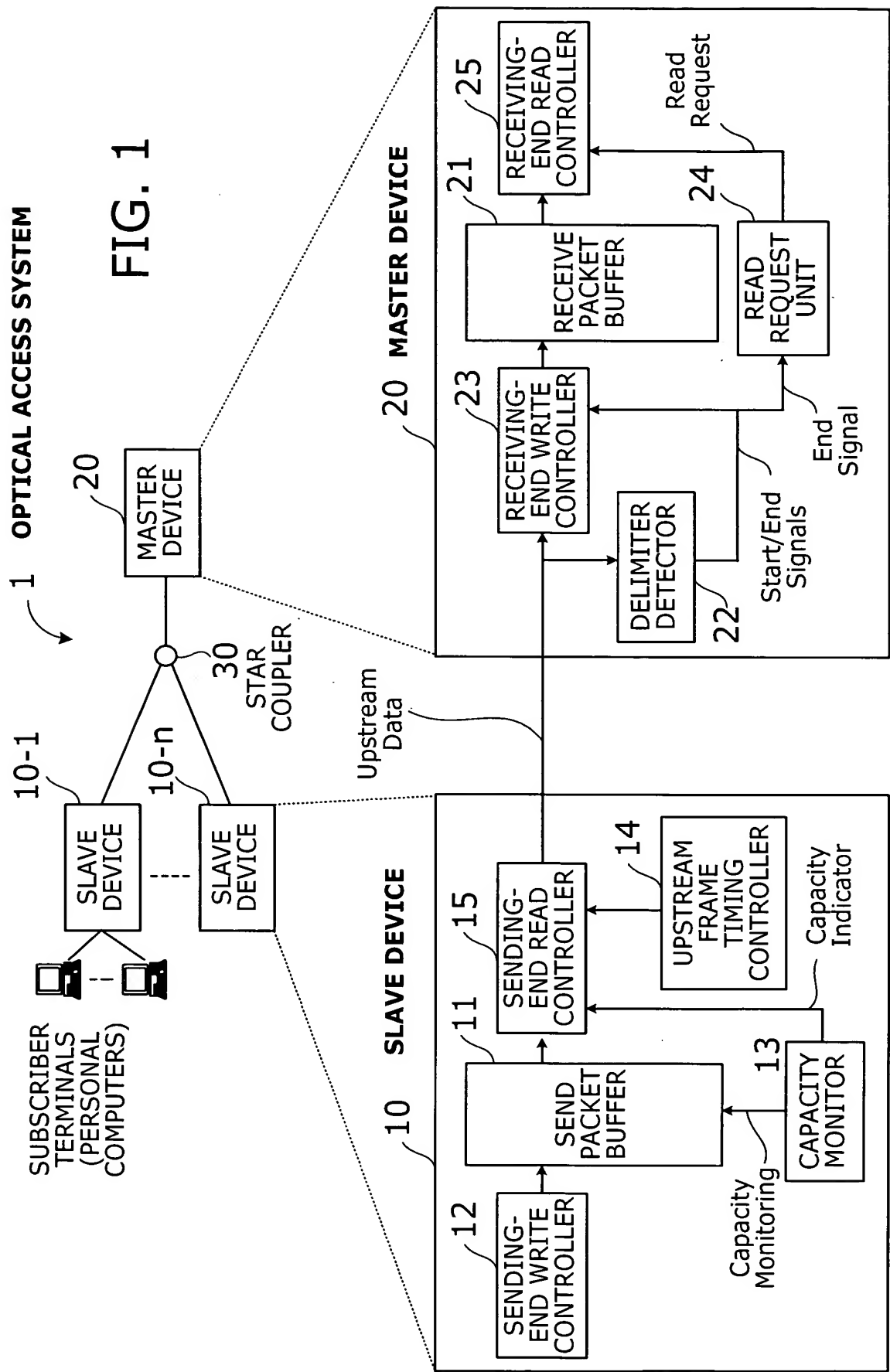


FIG. 1

1 OPTICAL ACCESS SYSTEM



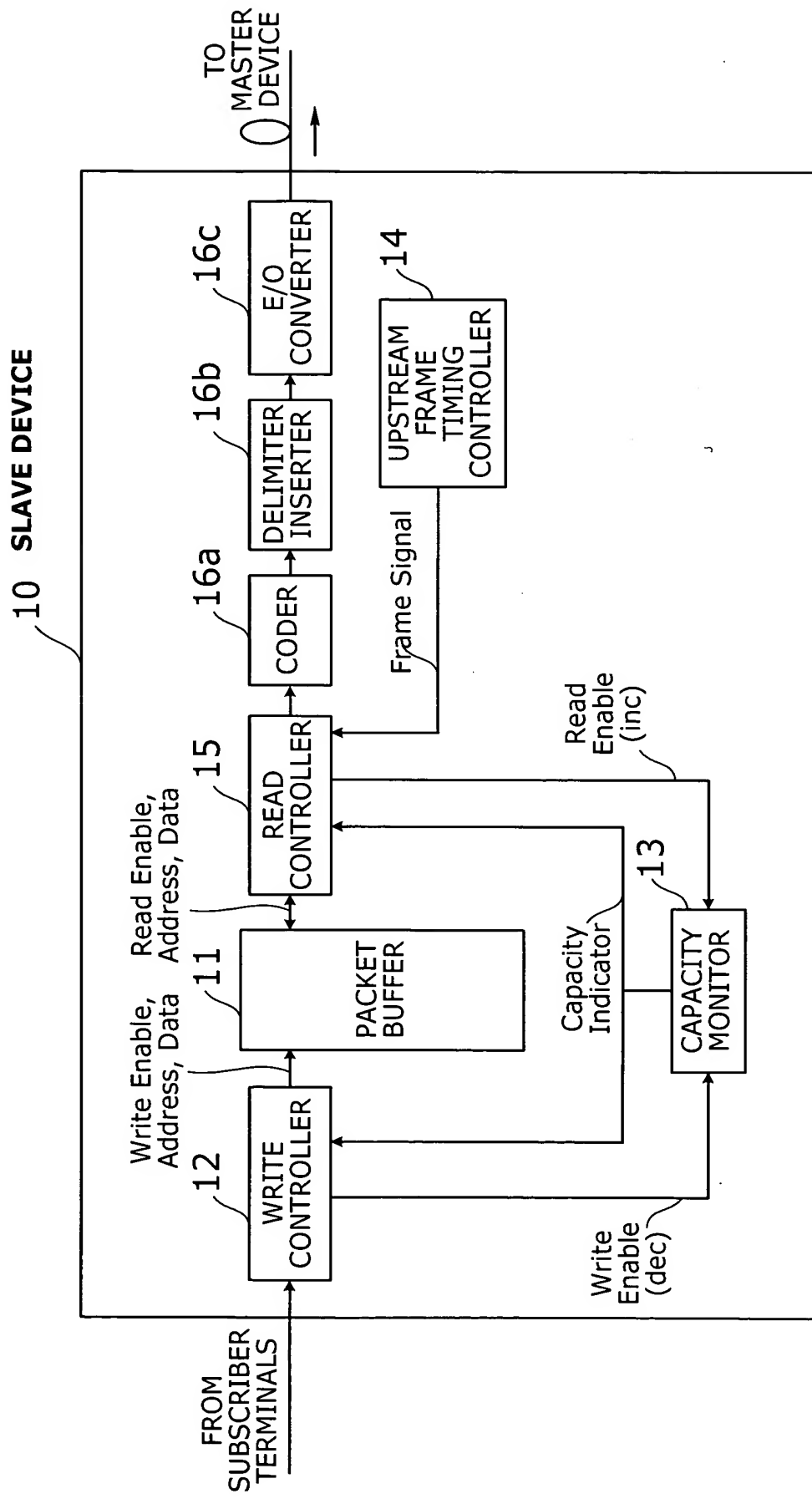
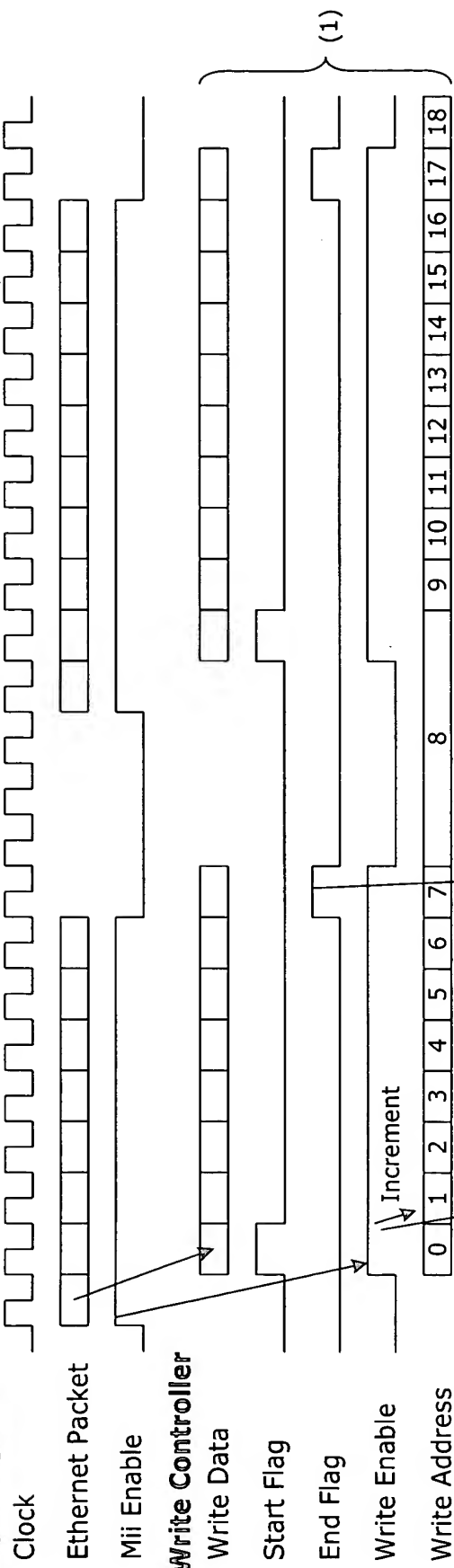


FIG. 2

Input Signals



Capacity Monitor

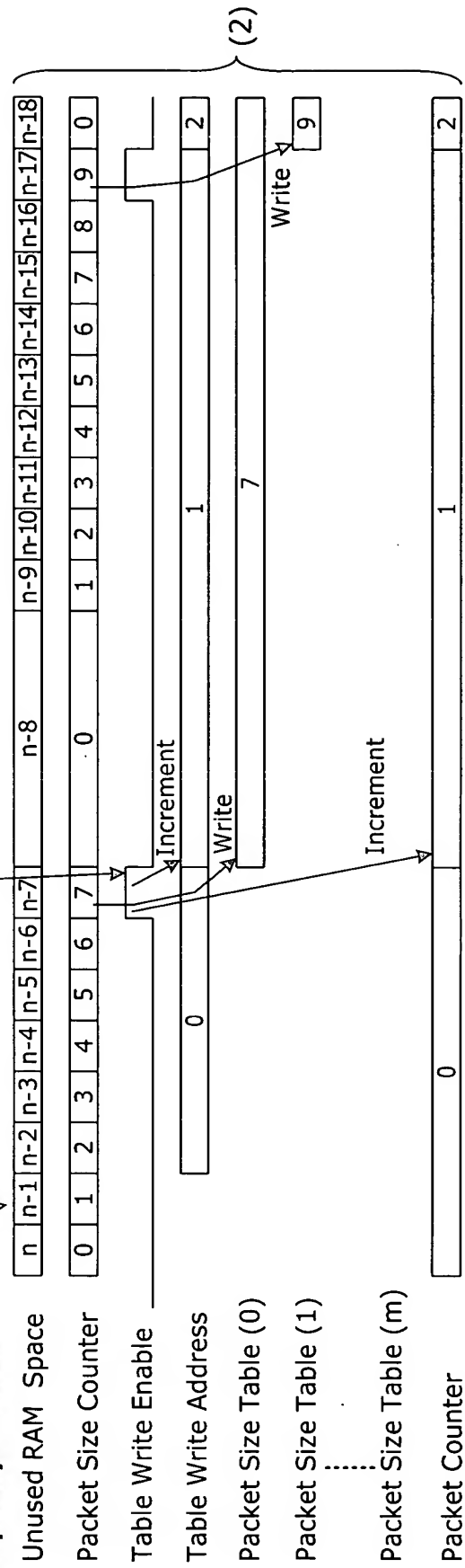


FIG. 3

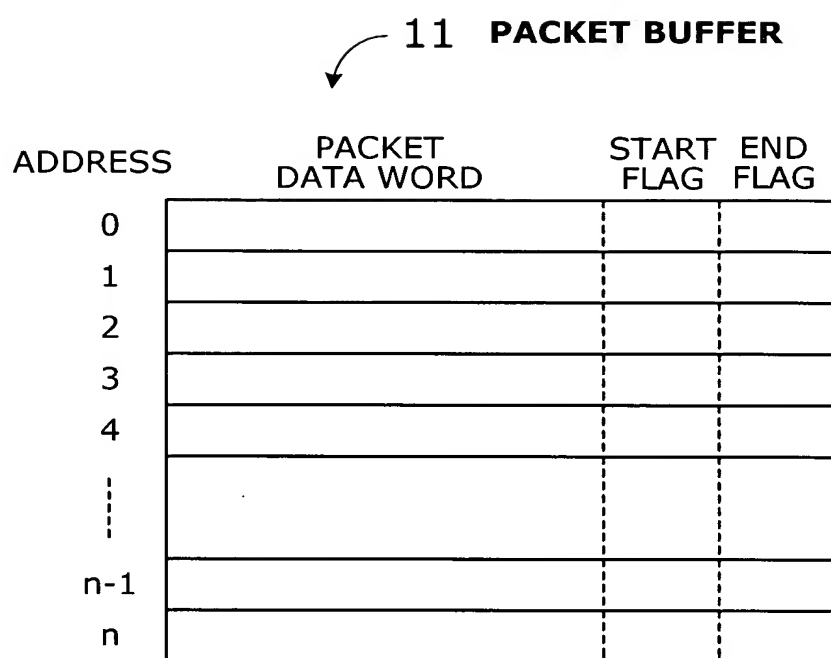


FIG. 4

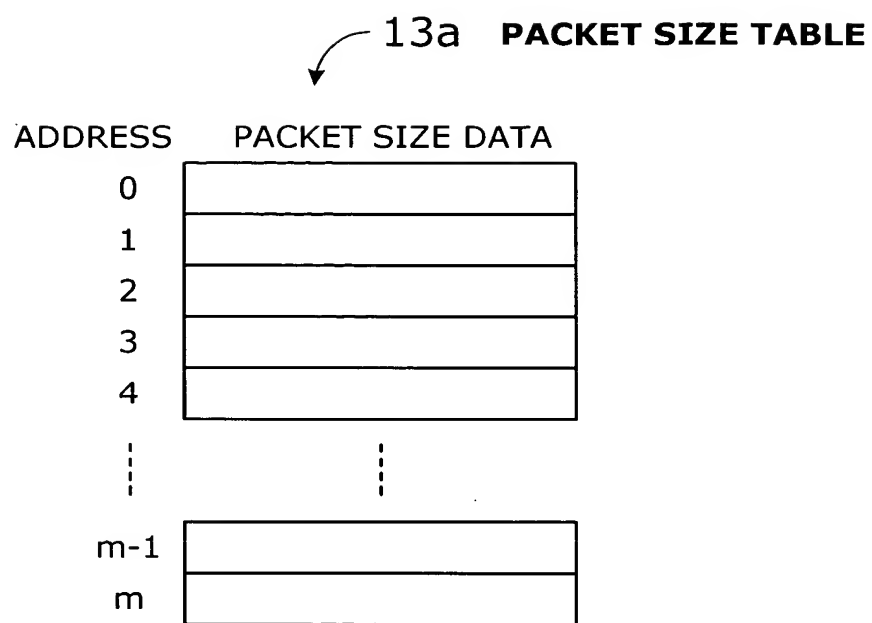


FIG. 5

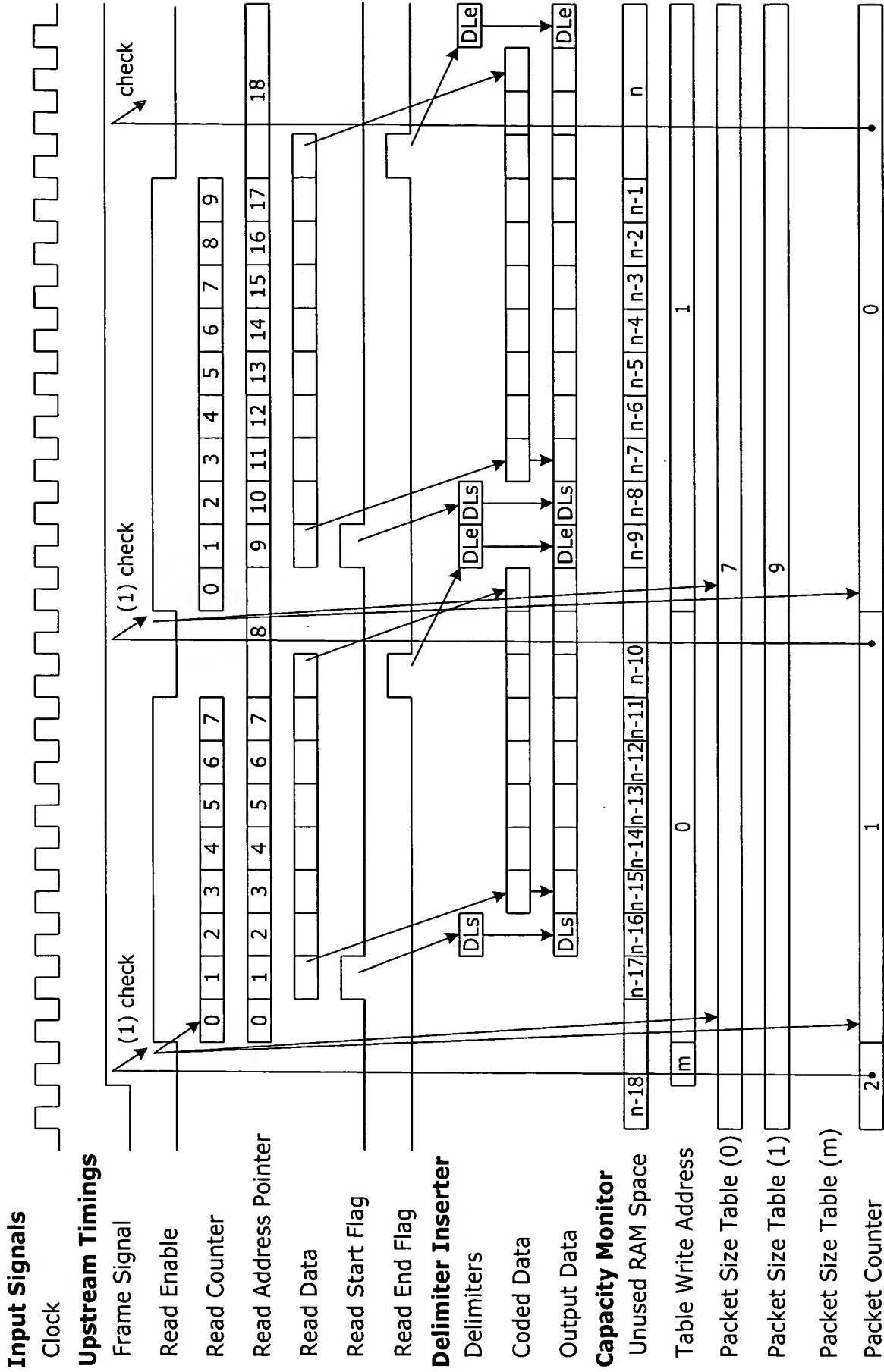


FIG. 6

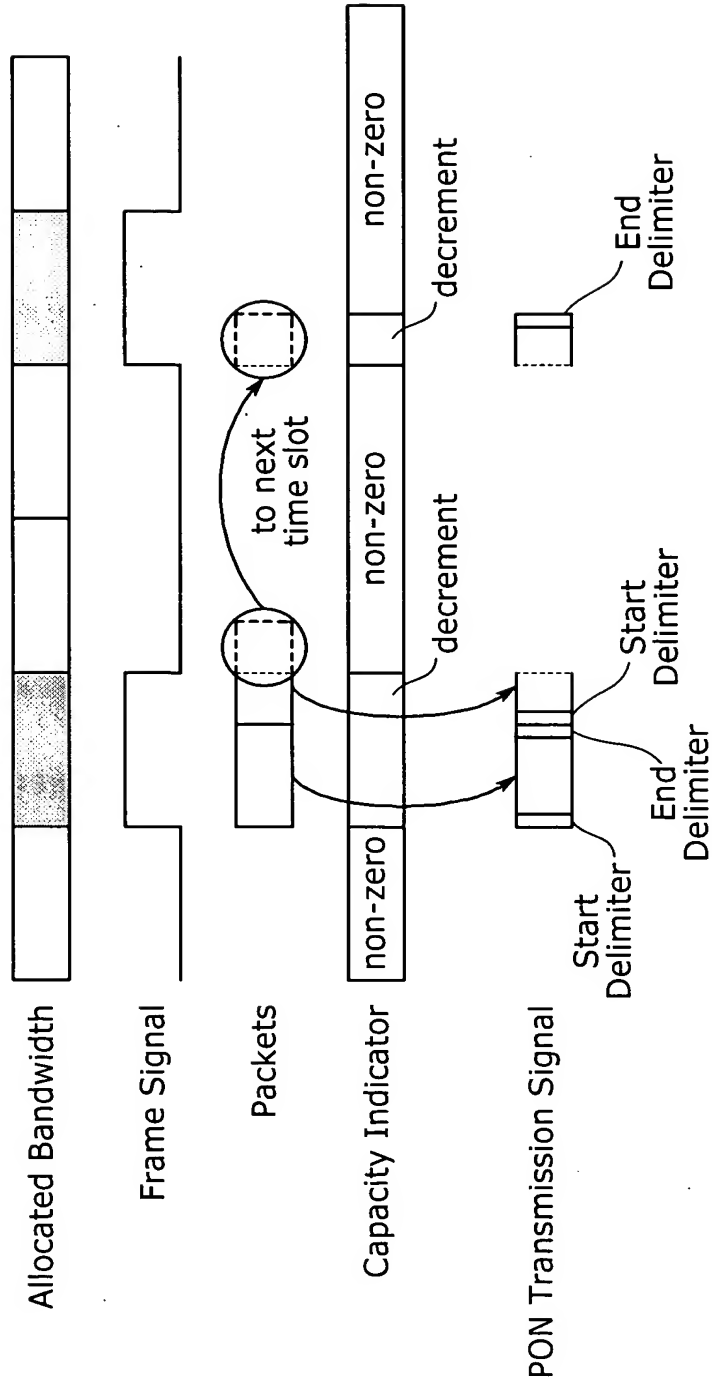


FIG. 7

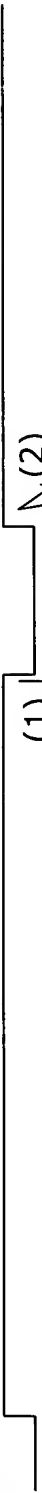
Input Signals

Clock



Upstream Timings

Frame Signal



Read Enable



Read Counter



Read Address Pointer



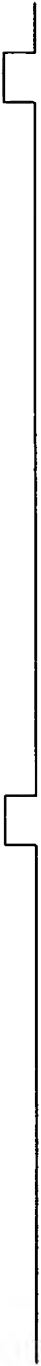
Read Data



Read Start Flag

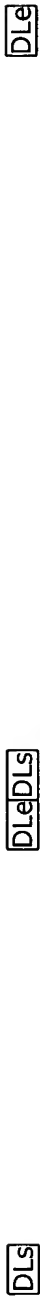


Read End Flag



Delimiter Inserter

Delimiters



Coded Data



Output Data



Capacity Monitor

Unused RAM Space



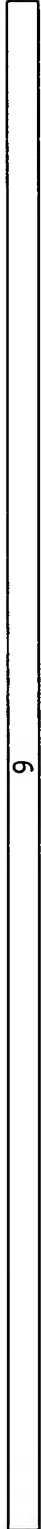
Table Write Address



Packet Size Table (0)



Packet Size Table (1)



Packet Size Table (m)



Packet Counter



FIG. 8

20 MASTER DEVICE

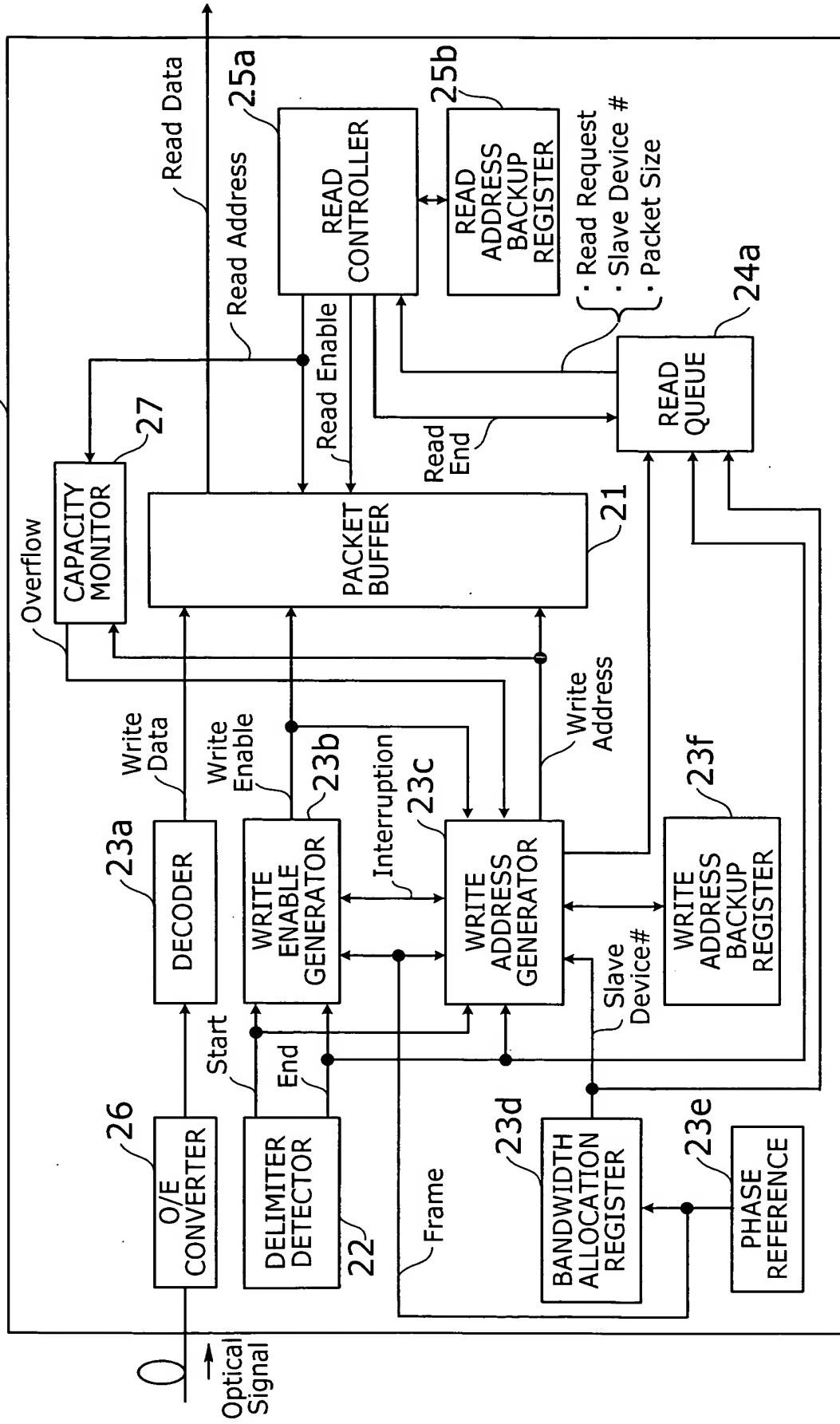


FIG. 9

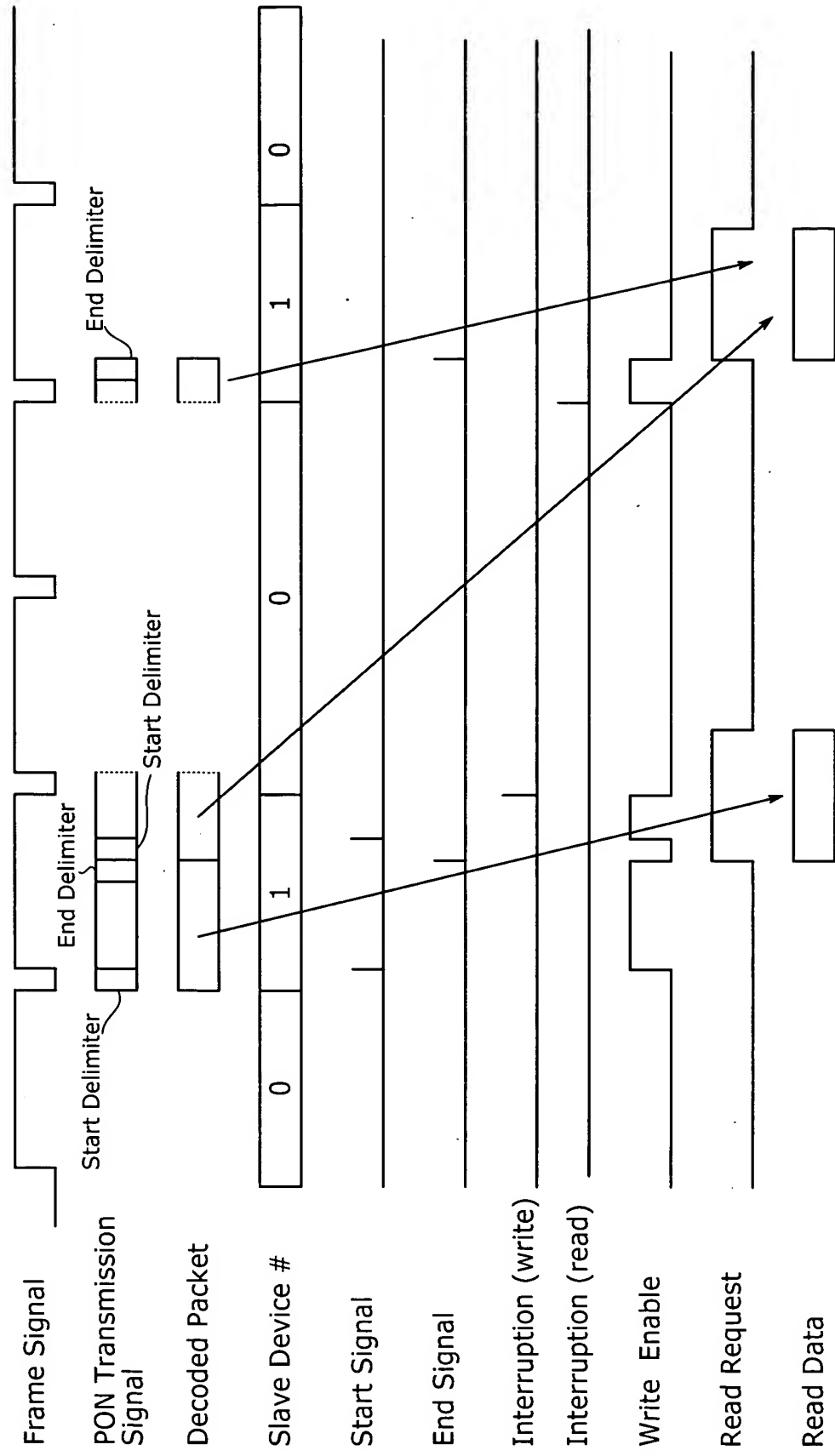


FIG. 10

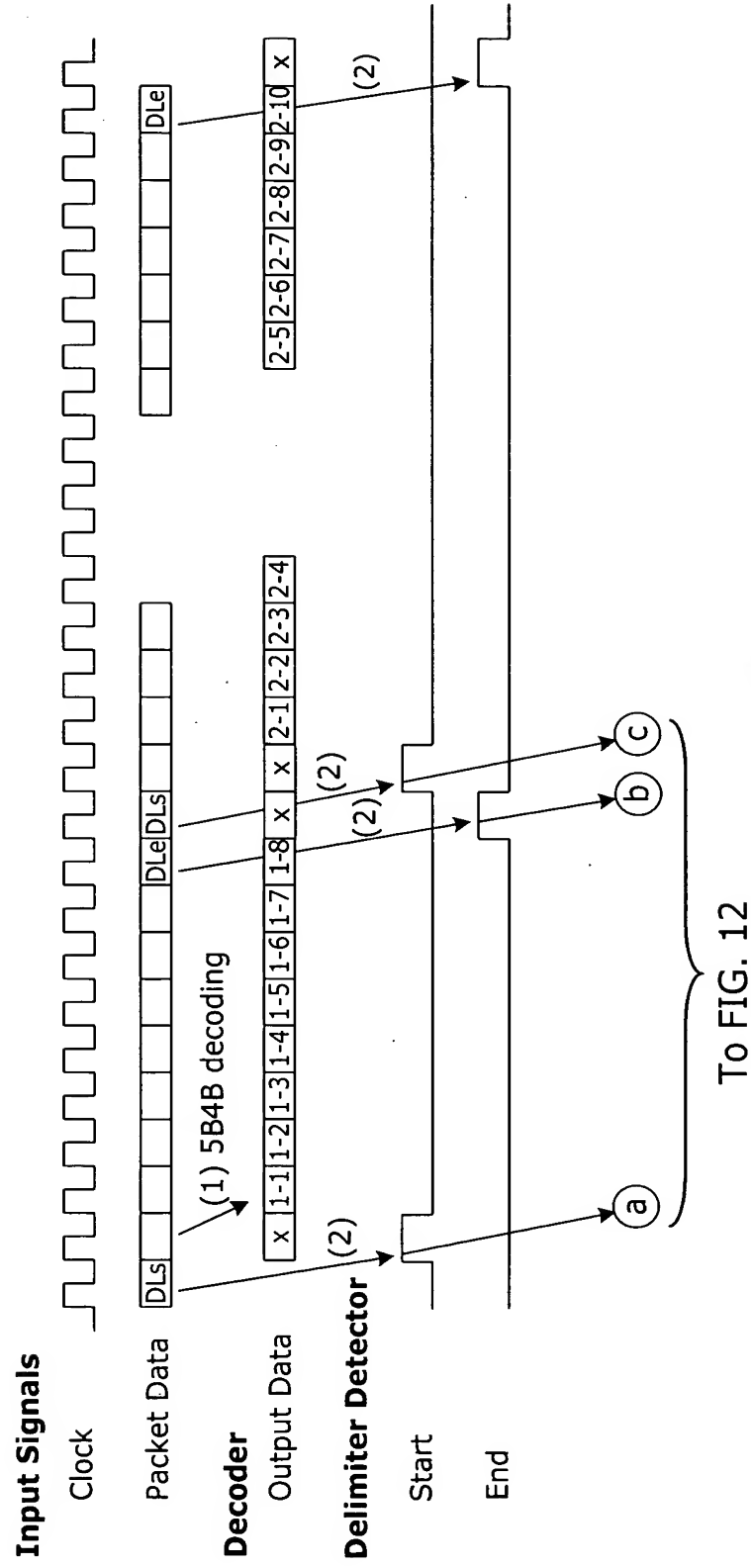


FIG. 11

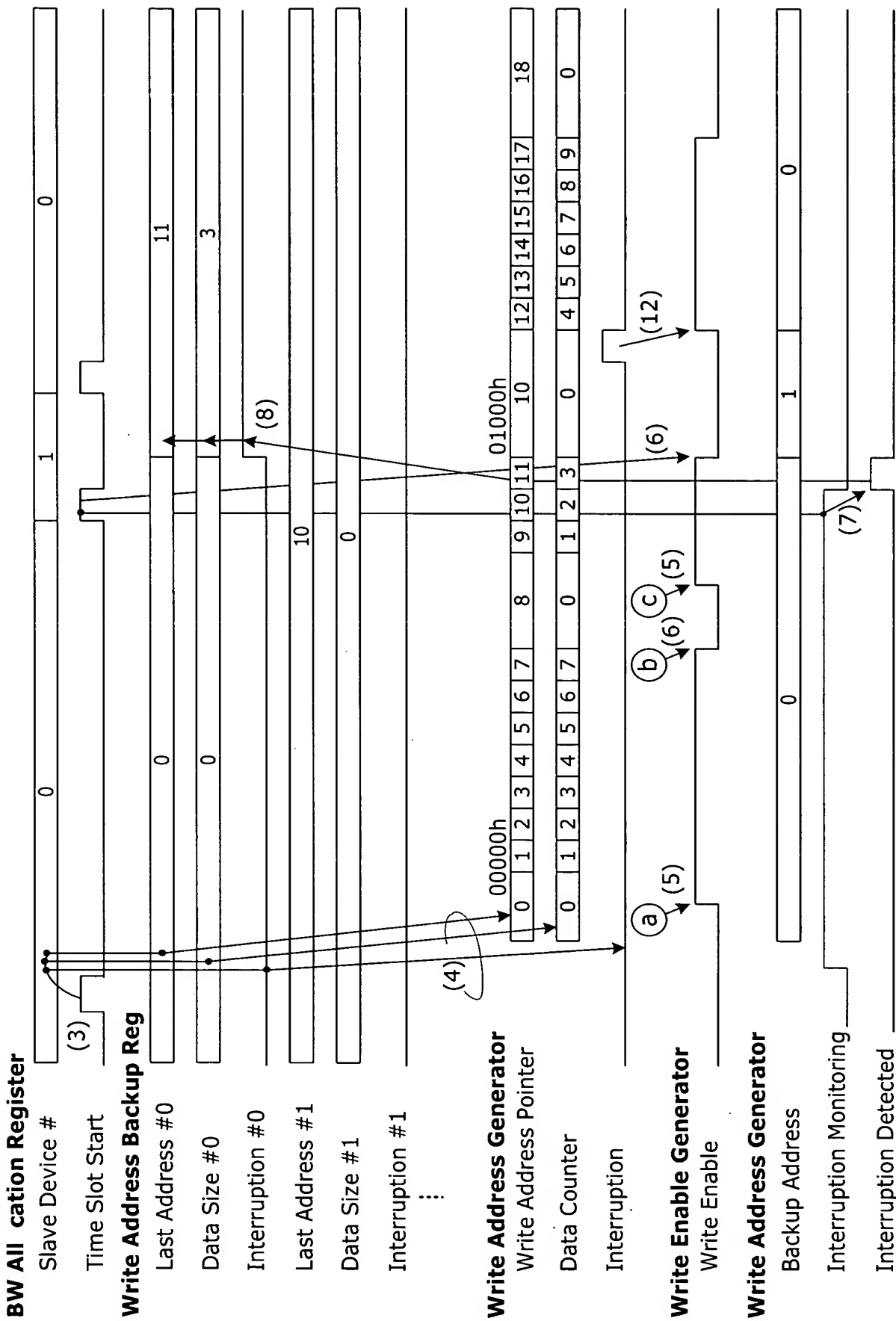


FIG. 12

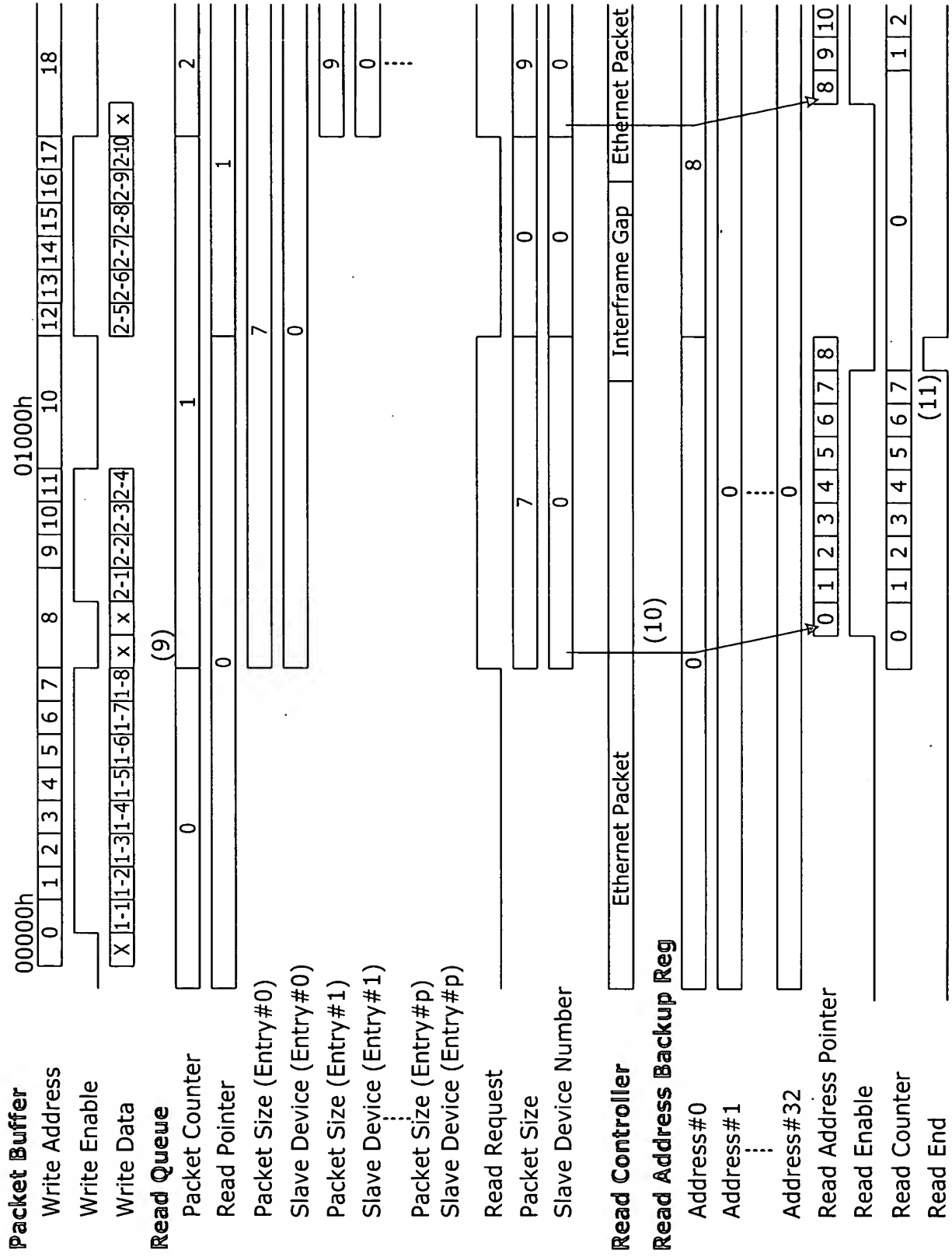


FIG. 13

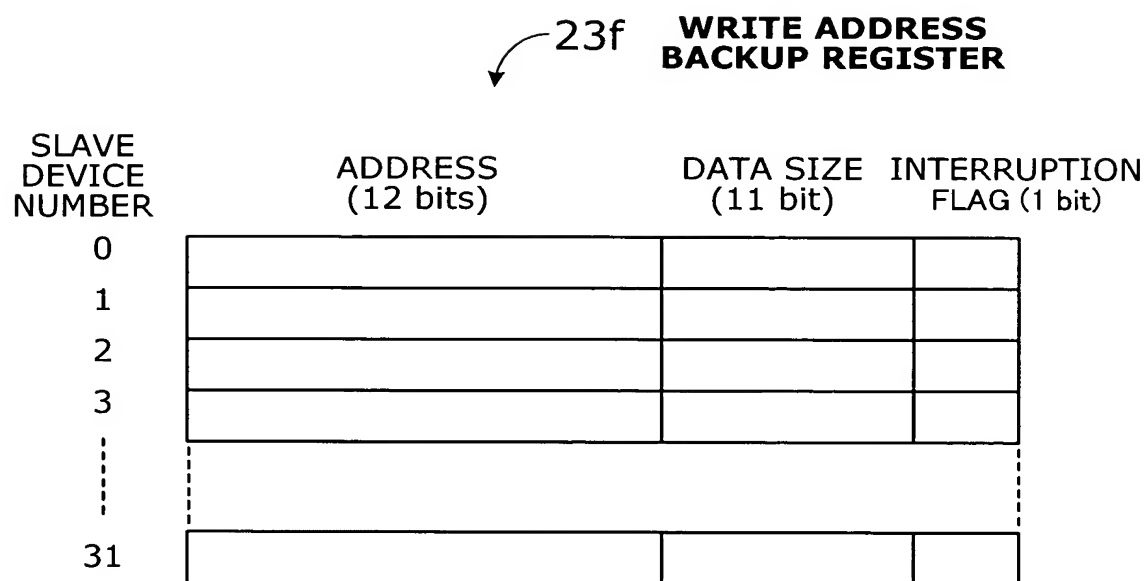


FIG. 14

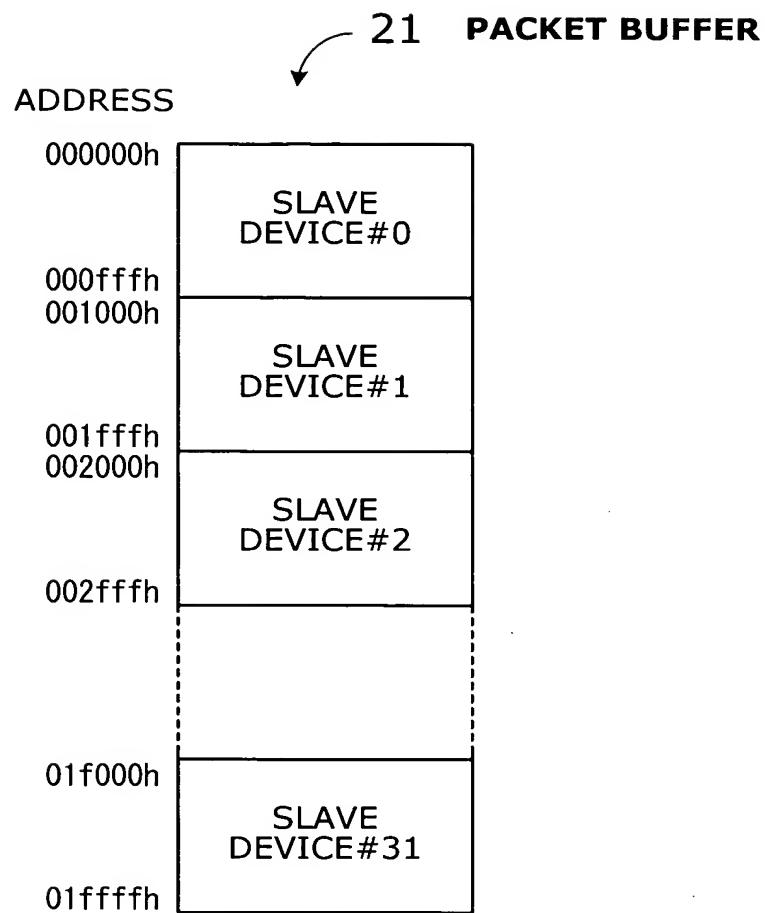


FIG. 15

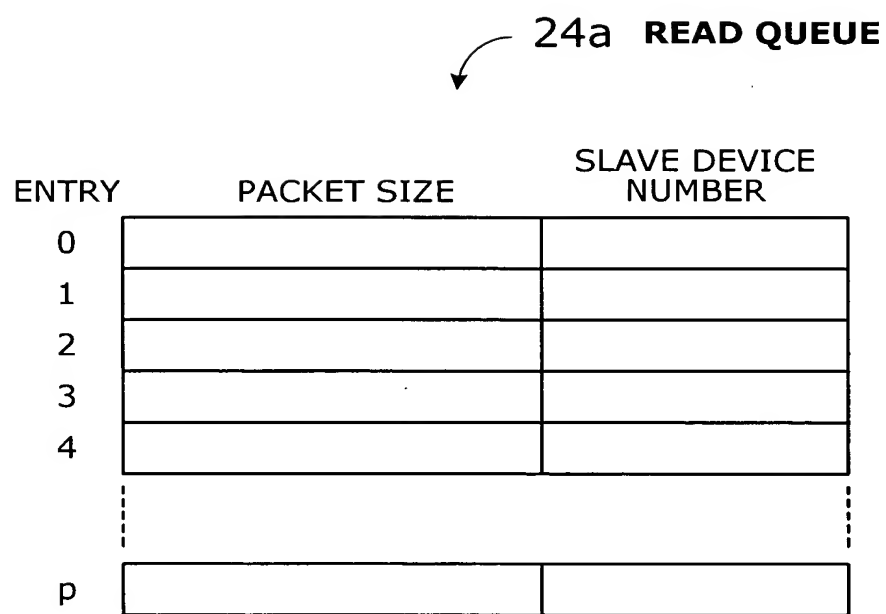
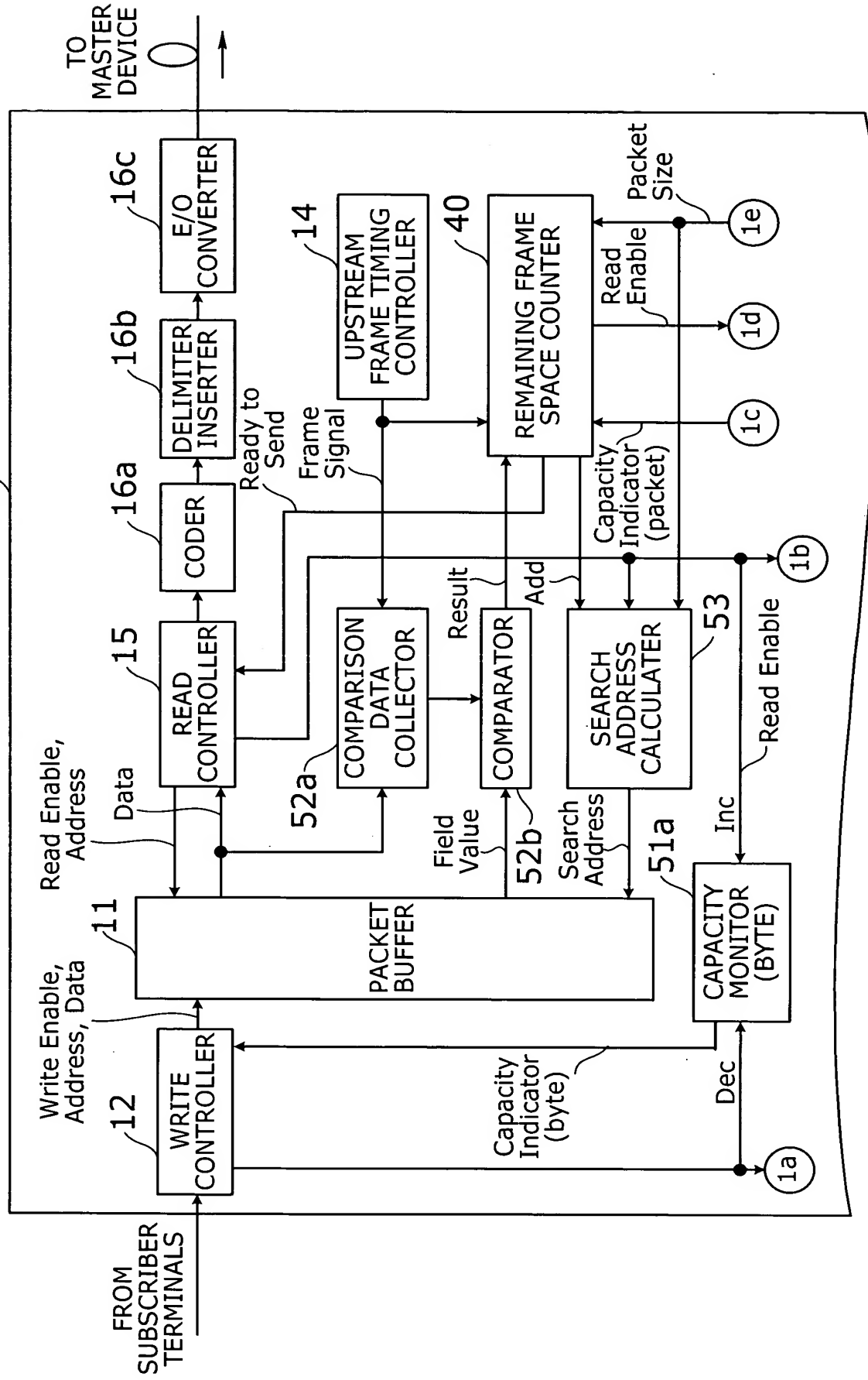


FIG. 16

FIG. 17

10a SLAVE DEVICE



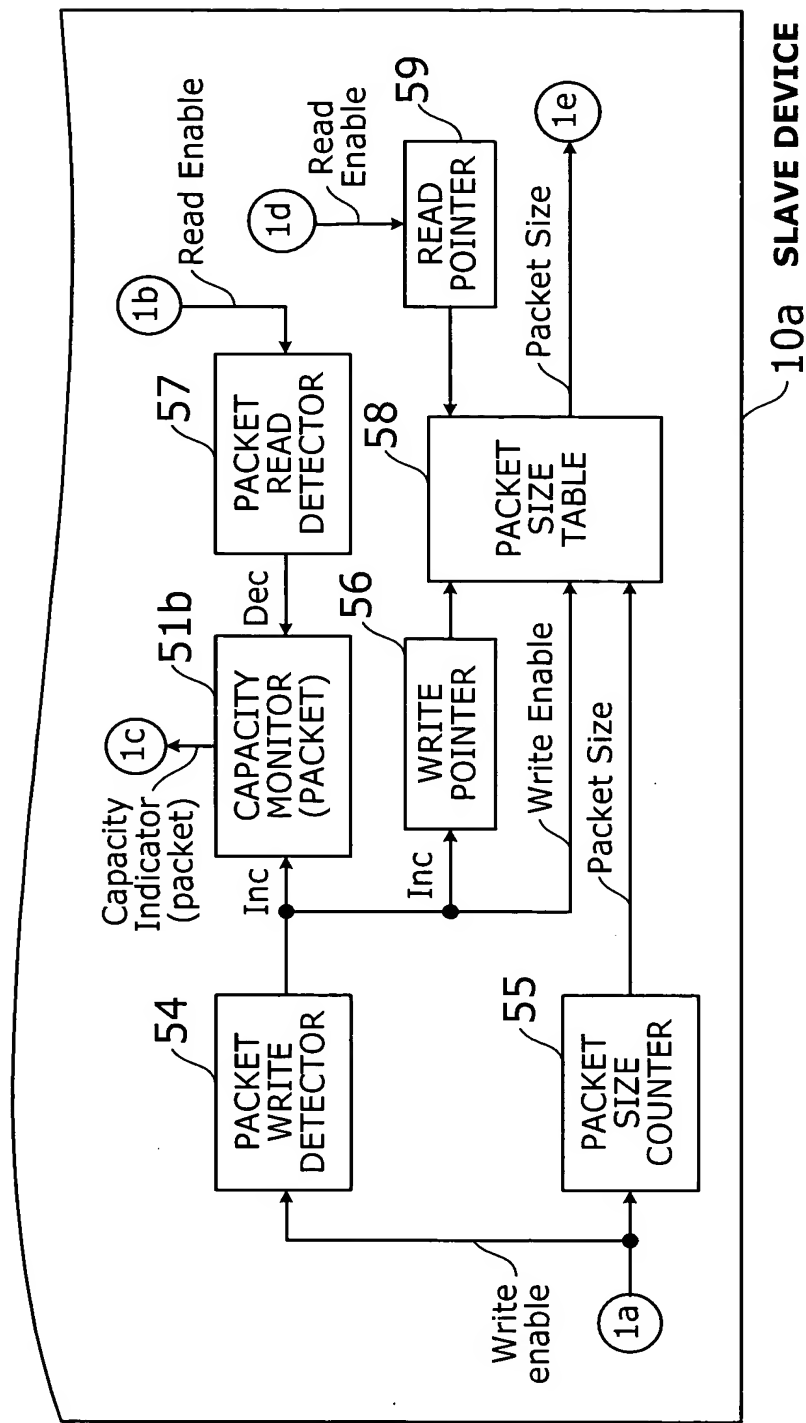


FIG. 18

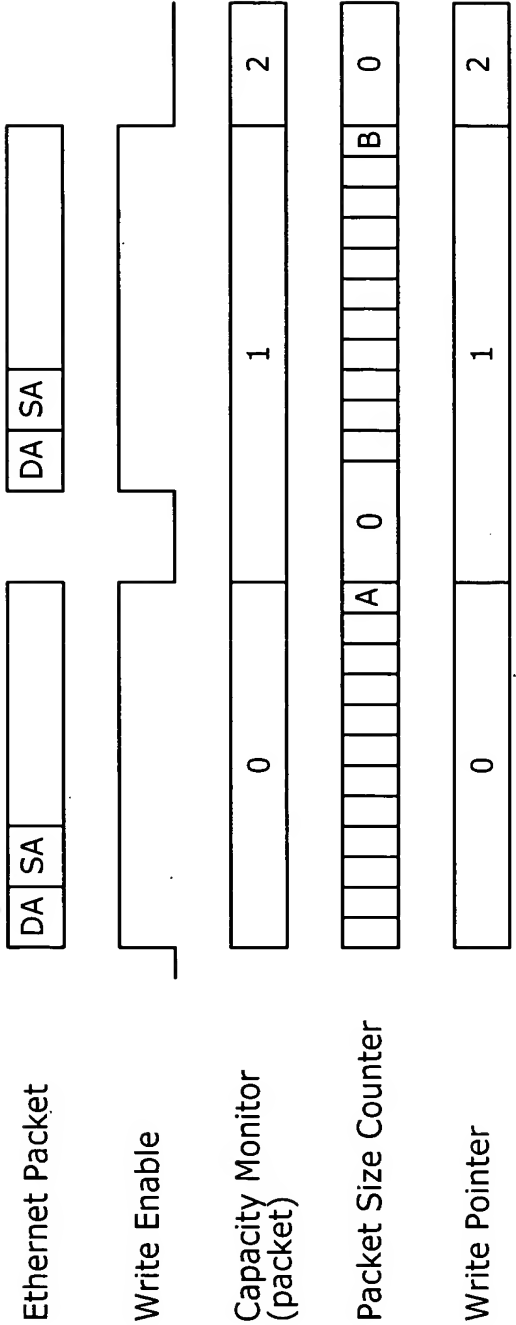


FIG. 19

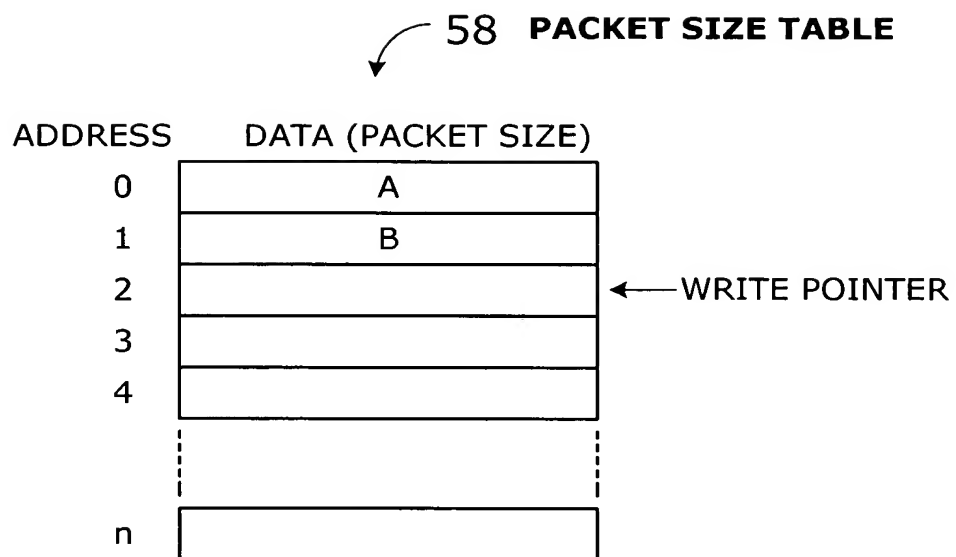


FIG. 20

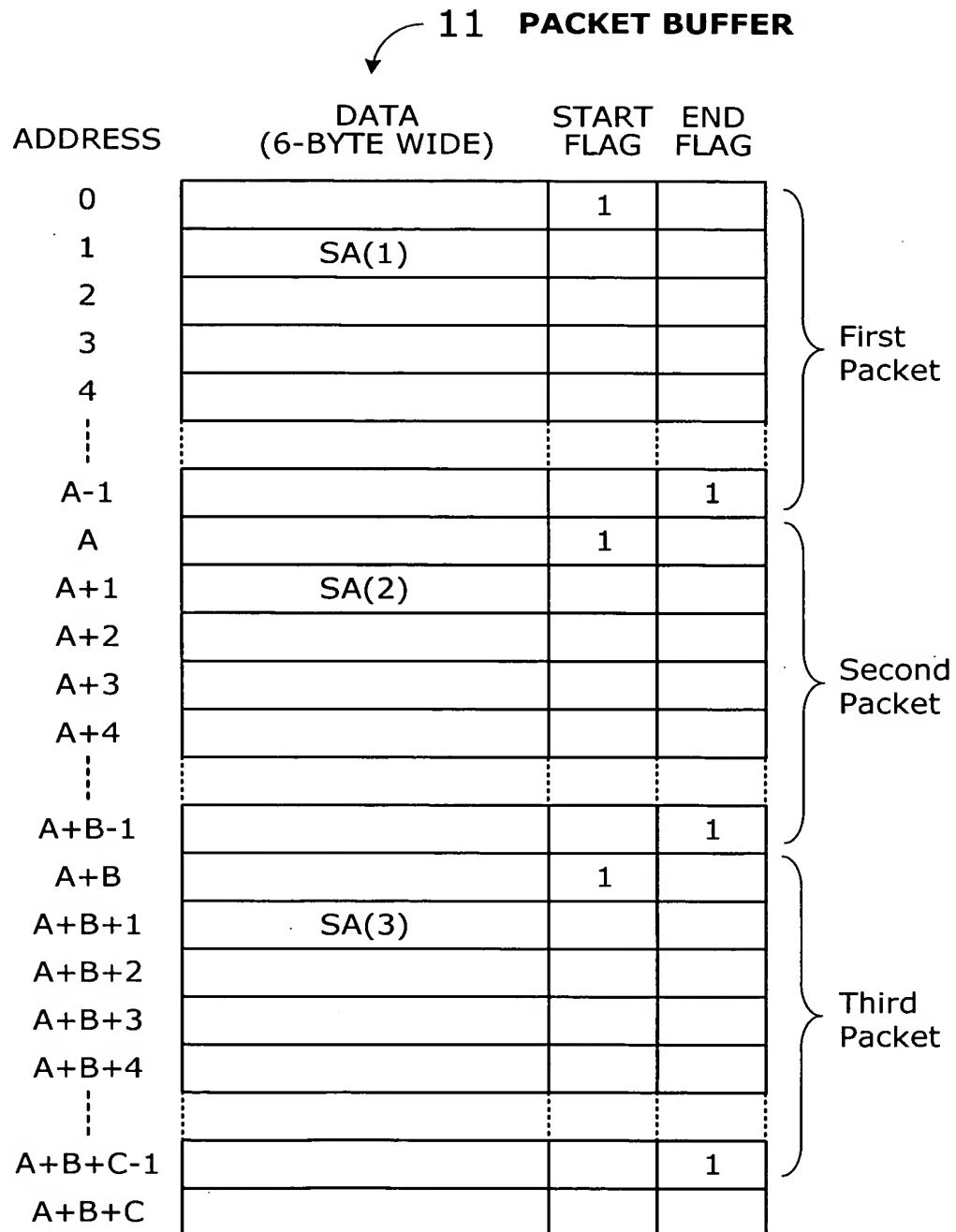
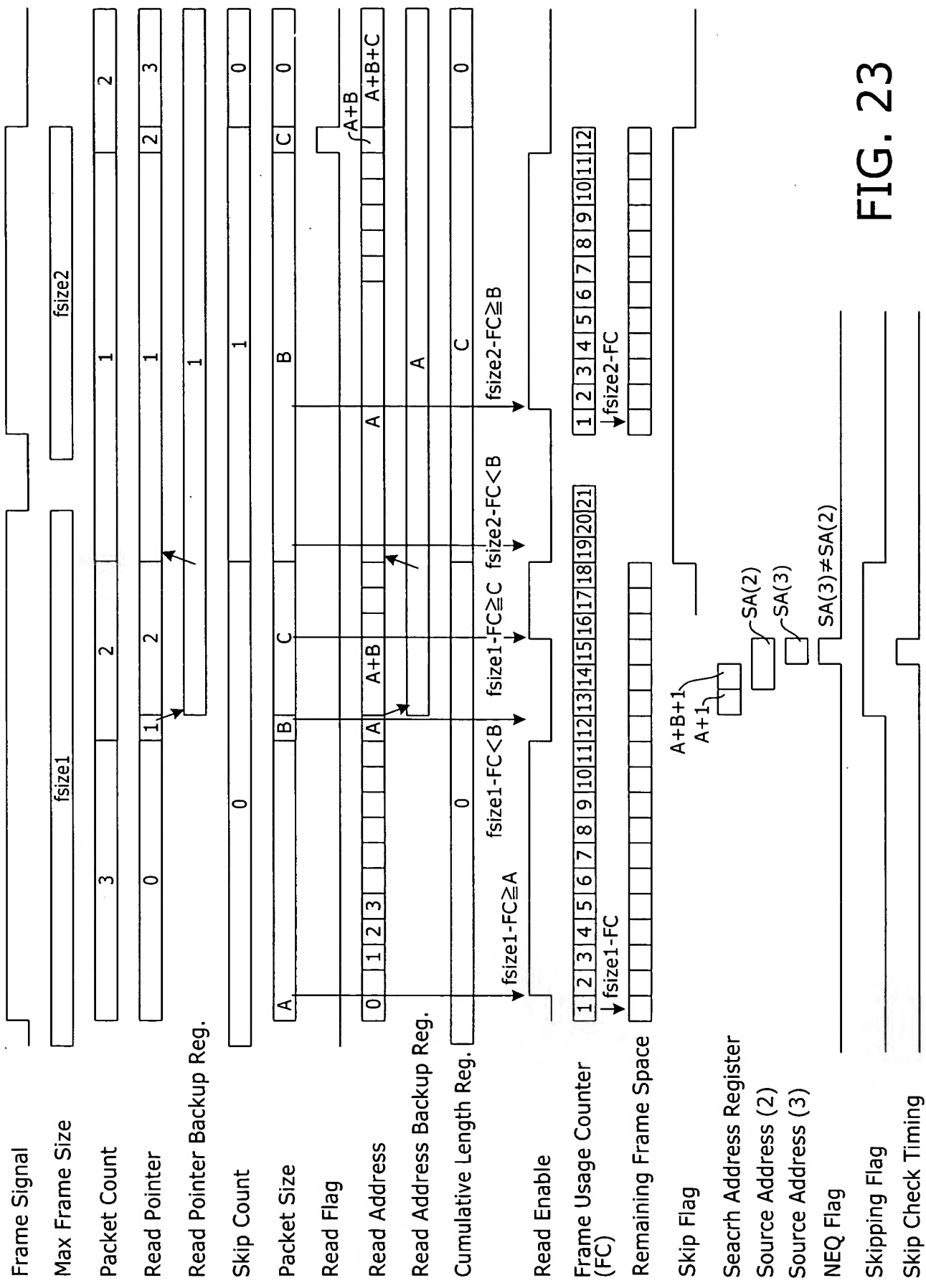


FIG. 21

58 PACKET SIZE TABLE

ADDRESS	DATA (PACKET SIZE)	READ FLAG
0	A	0
1	B	0
2	C	0
3		
4		
⋮		
n		

FIG. 22



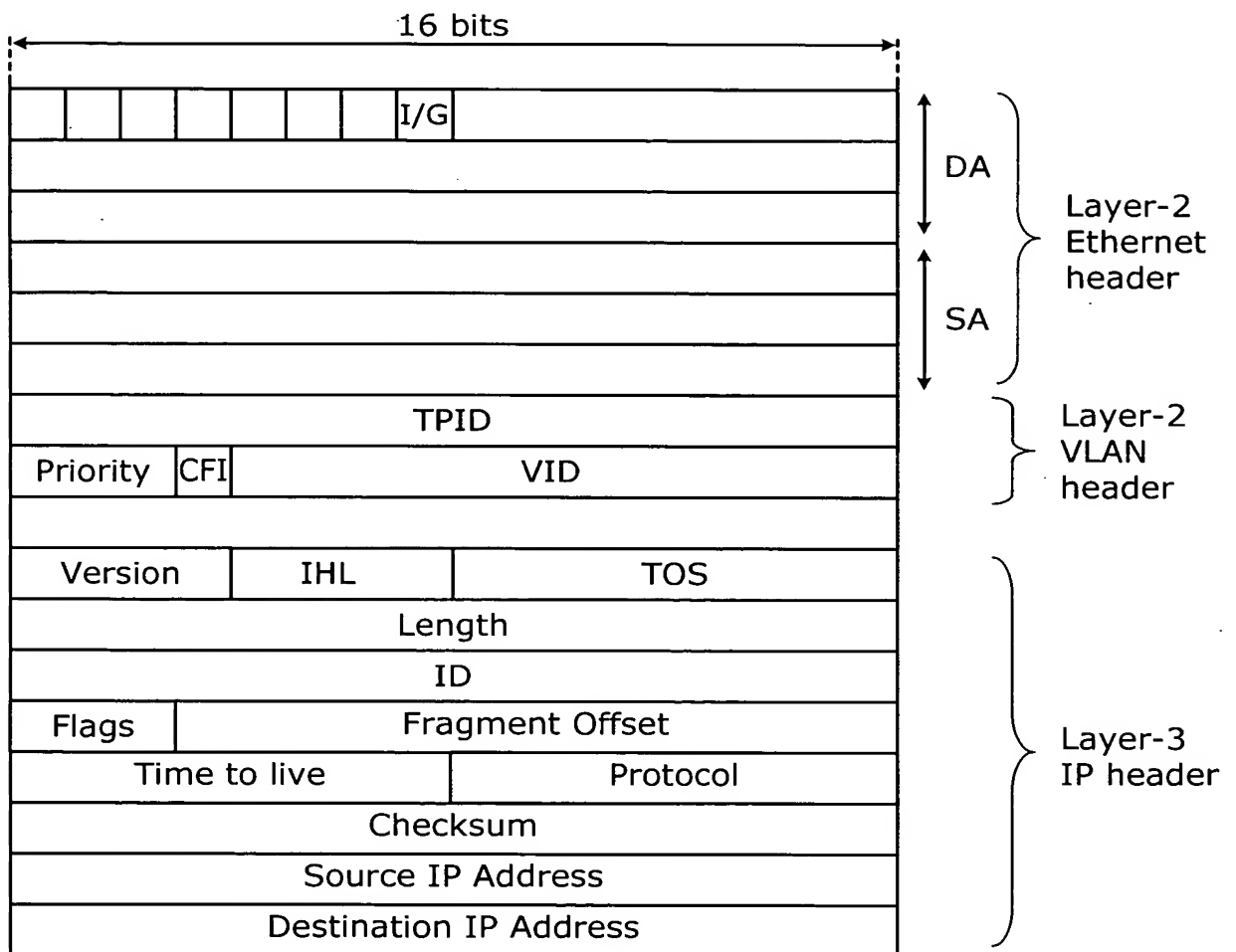


FIG. 24

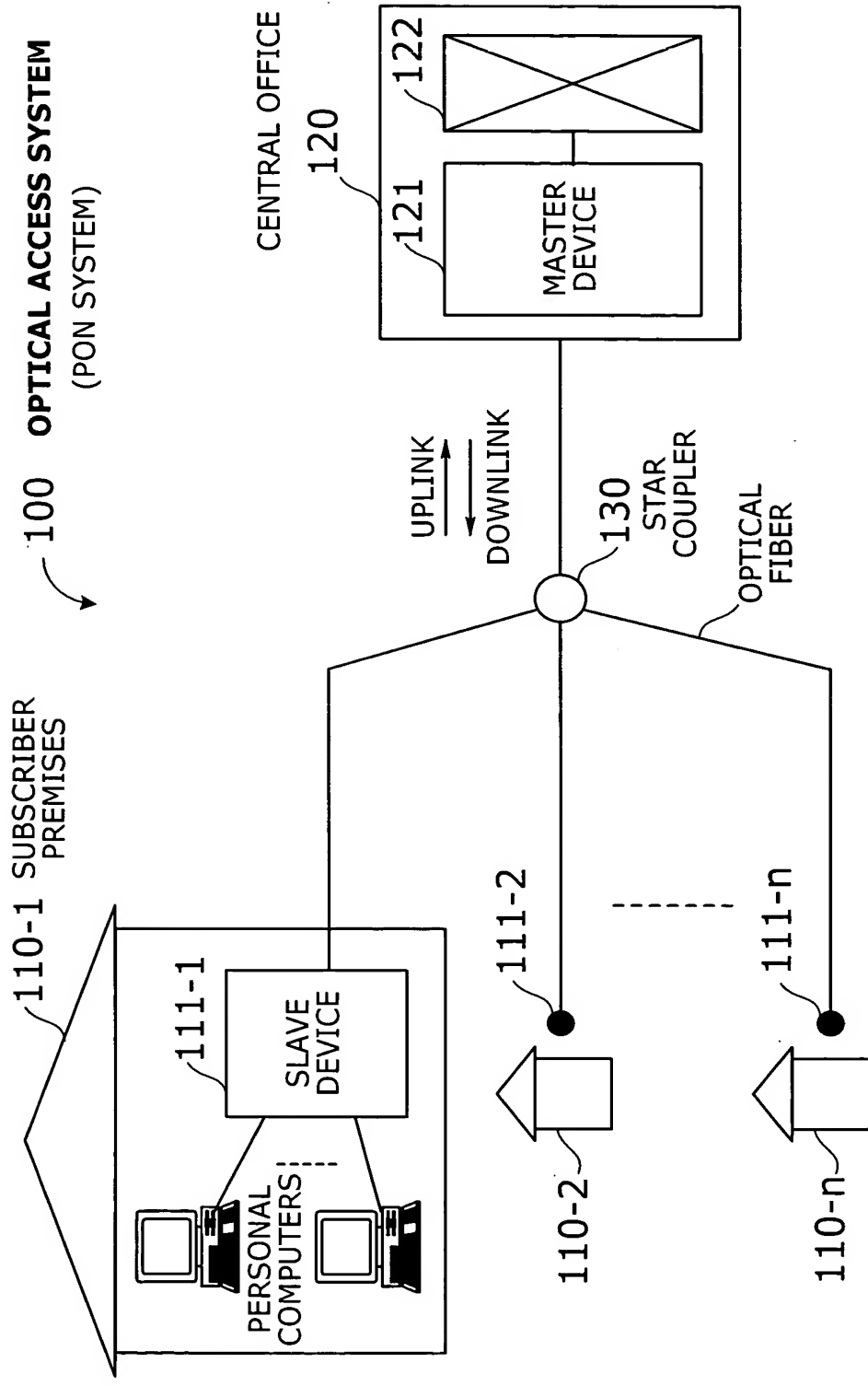
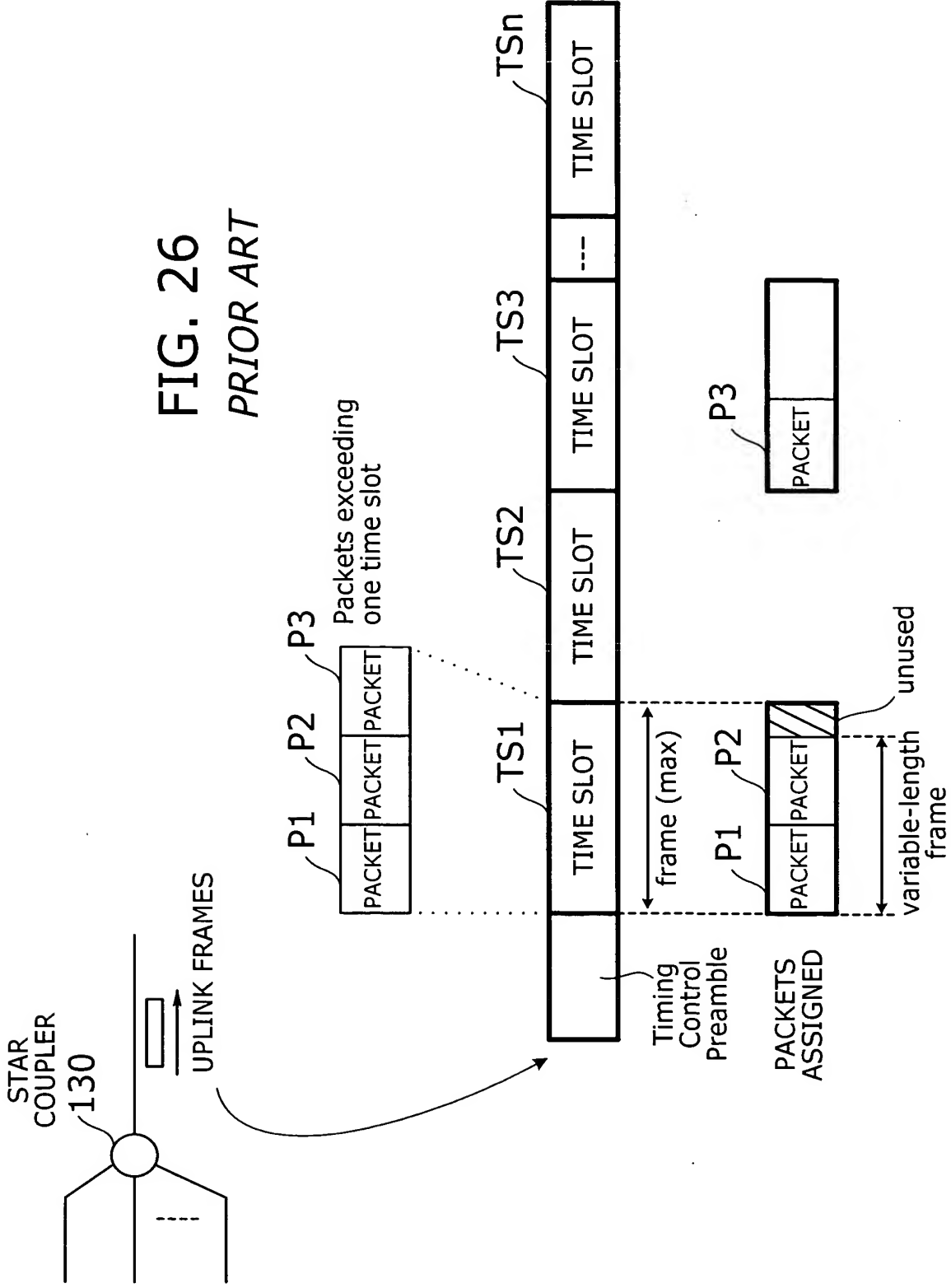


FIG. 25 PRIOR ART



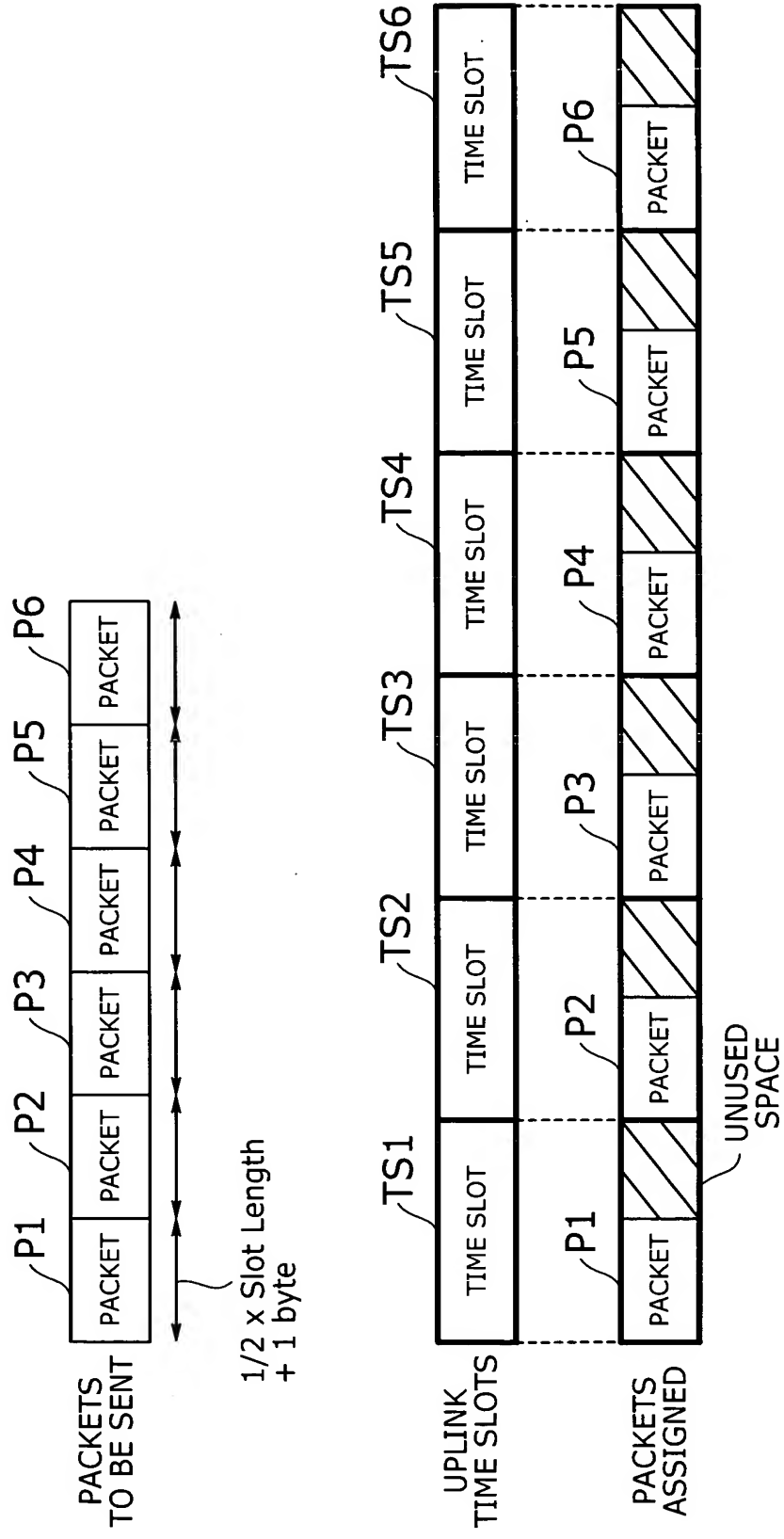


FIG. 27 *PRIOR ART*